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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/032,639	12/28/2001	Do-Young Lee	29926/38066	6899

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EXAMINER	
LAM, HUNG H	
ART UNIT	**PAPER NUMBER**
2615	

DATE MAILED: 11/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/032,639	LEE, DO-YOUNG	
	Examiner	Art Unit	
	Hung H. Lam	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 August 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The amendments, filed on 08/31/05, have been entered and made of record. Claims 1-16 are pending.

In view of the Applicant's amendment of Figs. 2-3, the objections are hereby withdrawn.

The title of the invention should be changed to " AN IMPROVED CMOS IMAGE SENSOR WHEREIN AN A/D CONVERTER EXECUTES AD CONVERSION AND GAMMA CORRECTION".

Response to Arguments

2. Applicant's arguments, see the remark on page 8, filed 08/31/05, with respect to the rejection(s) of claim(s) 1-6 under 102(e) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection in claims 1-6 and the newly added claims 7-16 are made.

The Applicants argue that Lee's US. filing date on Jun 6, 2002 is not conclusively available as a reference in according to the Applicant's priority date on Dec. 30, 2000. However, the Examiner has relied on the effective filling date of Lee's provisional applications that filed on Feb. 11, 2000. The Examiner quotes: " If application properly claims benefit under 35 U.S.C 119(e) to a provisional application, the effective filing date is the filing date of the provisional application for any claims which are fully supported under the first paragraph of 35 U.S.C 112

by the provisional application." See MPEP 706.02 (V) "Determining the Effective Filing Date of the Application" under (D).

Claim Rejections - 35 USC § 102

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

CLAIMS 5-6 ARE EXAMINED FIRST.

4. Claims 5-6 rejected under 35 U.S.C. 102(e) as being anticipated by Lee (US-6,545,624).

With regarding to **claim 5**, Lee discloses a CMOS image sensor, comprising:

an image capturing means for capturing an analog image signal from an object (Fig. 3; Pixel Array 307);

an analog-to-digital converter to convert the analog image signal to a digital image signal (Fig. 3; ADC 30; Col. 3, Ln. 54-59); and

a ramp signal generator providing a ramp signal to the analog-to-digital converter as a reference voltage signal (Fig. 3; comparator 310 compares pixel signal 306 with reference ramp signal 305), said ramp signal generator including: a first switch connected to a gain voltage (Fig. 4A; switch S1 is coupled to V_GAIN);

a plurality of second switches connected in parallel to the first switch (Fig. 4A; see switches S2-SM);

a plurality of capacitors connected to the second switches (capacitors CI2-CIM are connected to Switches S2-SM respectively);

a third switch connected between the first switch and a ground voltage level (Switch T1 is connected between first switch S1 and Vss which is commonly used in the art as ground);

a fourth switch commonly connected to the plurality of capacitors and connected to a reset voltage (SW1 is connected between plurality of capacitors CI2-CIM and V_RESET);

a fifth switch connected to the plurality of capacitors (SW2 is coupled to capacitors CI2-CIM);

an amplifying means for receiving the reset voltage and receiving the gain voltage via the fifth switch for outputting the ramp signal (see the connections between V_RESET, V_GAIN, SW2, and amplifier 401);

a sixth switch connected in parallel to the amplifying means (SW4); and

a capacitor connected in parallel to the sixth switch (C2).

With regarding to **claim 6**, Lee discloses the CMOS sensor wherein the plurality of capacitors and the second switches in the ramp signal generator are selectively connected to each other in response to control signals from a digital controller in the CMOS image sensor (Fig. 4A; Col. 3, Ln. 60-64; Col 4, Ln. 51-55; the plurality of capacitors CI2-CIM inherently connect to the second switches S2-SM in response to clock CLK1 and CLK2).

Claim Rejections - 35 USC § 103

5. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

6. Claims 1 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (US-6,545,624) in view of Eikichi (JP08-190363).

With regarding to **claim 1**, Lee discloses a CMOS image sensor, comprising:

an image capturing means for converting light incident upon a photo-sensitive area to an analog image signal (Fig. 3; Pixel Array 307);

an analog-to-digital converter for converting the analog image signal to a digital image signal (Fig. 3; ADC 30; Col. 3, Ln. 54-59); and

a ramp signal generator for providing a ramp signal to the analog-to-digital converter as reference voltage signal (Fig. 3; comparator 310 compares pixel signal 306 with reference ramp signal 305), the ramp signal generator including: a plurality of capacitors and switches (Fig. 4A; Col. 4, Ln. 30-43);

an amplifier coupled to the plurality of capacitors and switches for receiving gain and reset voltages from external circuitry (see Fig. 4A; amplifier 401, Capacitors CI1-IM, Switches S1-SM, SW1-SW4, T1-TM, V_GAIN and V_RESET); and

capacitance controlling means coupled in parallel to at least one of the plurality of capacitors in the ramp signal generator in order to adjust the ramp signal for a gamma correction (Col. 1, Ln. 49-60; Col. 4, Ln. 58-67; Col. 6, Ln. 30-50 wherein Lee teaches the transition slope increasing dynamic range which commonly known in the art for a direct linking to gamma correction).

However, Lee fails to explicitly disclose that capacitance controlling means adjusts the ramp signal for a gamma correction.

In the same field of endeavor, Eikichi teaches a video signal processing device for providing exact gamma correction in a dynamic gamma processing circuit by enlarging the dynamic range of the input signal of an A/D conversion circuit (Abstract; Effect of the Invention; [0025]). In light of the teaching from Eikichi, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device of Lee by having a dynamic gamma processing circuit as claimed by Eikichi in order to adjusts the ramp signal for increasing the dynamic range and thereby improving the S/N ratio and providing the exact gamma correction in a dynamic gamma processing circuit (Eikichi; Abstract; Effect of the Invention; [0025]).

With regarding to **claim 7**, Lee discloses the CMOS image sensor, comprising:

a converter (ADC) for receiving an inputted analog data and a ramp signal to thereby converting the inputted analog data into a digital data throughout a correlated double sampling (Fig. 5; Col. 3, Ln. 14-25; Col. 5, Ln. 51- Col. 6, Ln. 5); and

Lee further teaches a ramp signal generator for providing the ramp signal, which is adjustable so that different ramp voltage slopes can be tailored for a specific application (Col. 4, Ln. 30-67; Col. 6, Ln. 30-50 wherein Lee teaches the transition slope increasing dynamic range which commonly known in the art for a direct link to gamma correction).

However, Lee fails to explicitly disclose converting the inputted analog data into a digital data throughout a gamma correction and providing the ramp signal which is adjusted for the gamma correction.

In the same field of endeavor, Eikichi teaches a video signal processing device for providing exact gamma correction in a dynamic gamma processing circuit by enlarging the dynamic range of the input signal of an A/D conversion circuit (Abstract; Effect of the Invention; [0025]). In light of the teaching from Eikichi, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device of Lee by having a dynamic gamma processing circuit as claimed by Eikichi in order to adjusts the ramp signal for increasing the dynamic range and thereby improving the S/N ratio and providing the exact gamma correction in a dynamic gamma processing circuit (Eikichi; Abstract; Effect of the Invention; [0025]).

7. Claims 1-4, 7-9 and 13-16 rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (US-6,545,624) in view of Tomoaki (JP01-094725).

With regarding to **claim 1**, Lee discloses a CMOS image sensor, comprising:

an image capturing means for converting light incident upon a photo-sensitive area to an analog image signal (Fig. 3; Pixel Array 307);

an analog-to-digital converter for converting the analog image signal to a digital image signal (Fig. 3; ADC 30; Col. 3, Ln. 54-59); and

a ramp signal generator for providing a ramp signal to the analog-to-digital converter as reference voltage signal (Fig. 3; comparator 310 compares pixel signal 306 with reference ramp signal 305), the ramp signal generator including: a plurality of capacitors and switches (Fig. 4A; Col. 4, Ln. 30-43);

an amplifier coupled to the plurality of capacitors and switches for receiving gain and reset voltages from external circuitry (see Fig. 4A; amplifier 401, Capacitors CI1-IM, Switches S1-SM, SW1-SW4, T1-TM, V_GAIN and V_RESET); and

capacitance controlling means coupled in parallel to at least one of the plurality of capacitors in the ramp signal generator in order to adjust the ramp signal for a gamma correction (Col. 1, Ln. 49-60; Col. 4, Ln. 30-67).

However, Lee fails to explicitly disclose that capacitance controlling means adjusts the ramp signal for a gamma correction.

In the same field of endeavor, Tomoaki teaches an A/D converter for converting video analog to digital signal (abstract). Tomoaki further teaches that the A/D converter is capable of simultaneously executing gamma correction and A/D conversion in order to eliminate unnecessary external correction circuit and thereby reducing the cost. In light of the teaching from Tomoaki, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device of Lee to adjusts the ramp signal for a gamma correction in order to simultaneously executing gamma correction and A/D conversion as claimed by Tomoaki. The modification thus simplifying the circuit design and reducing the cost (Tomoaki; abstract).

With regarding to **claim 2**, Lee in view of Tomoaki discloses the CMOS image sensor wherein the plurality of switches (Lee: S1-SM,T1-TM,SW1-SW4) in the ramp signal generator are selectively operated in response to control signals from a digital controller in the CMOS

image sensor (Lee: Fig. 4A; Control signal CLK1 and CLK2; Col. 3, Ln. 60-64; Col 4, Ln. 51-55).

With regarding to **claim 3**, Lee in view of Tomoaki discloses the CMOS image sensor wherein the capacitance controlling means includes the plurality of capacitors and the plurality of switches to selectively connect the plurality of capacitors to the amplifier in response to the control signals from the digital controller (Lee: Fig. 4A; Col. 3, Ln. 60-64; Col 4, Ln. 51-55; the plurality of capacitors CI1-CIM inherently connect to the amplifier 401 in response to clock CLK1 and CLK2).

With regarding to **claim 4**, Lee in view of Tomoaki discloses the CMOS image sensor further comprising: counting means for creating a digital counting value based on a result signal from a chopper comparator (Lee: Fig. 3, Counter 302; Col. 4, Ln. 1-3; Col. 4, Ln.16-29; counter 302 coupling to and storing counted value in to the storage 312 based on the output signal of comparator 308); and a latch circuit (Lee: Fig. 3; storage 312) for storing the digital counting value from the counting means (Lee: Col. 4, Ln. 22-24).

With regarding to **claim 7**, Lee discloses the CMOS image sensor, comprising:

a converter (ADC) for receiving an inputted analog data and a ramp signal to thereby converting the inputted analog data into a digital data throughout a correlated double sampling (Fig. 5; Col. 3, Ln. 14-25; Col. 5, Ln. 51- Col. 6, Ln. 5); and

Lee further teaches a ramp signal generator for providing the ramp signal, which is adjustable so that different ramp voltage slopes can be tailored for a specific application (Col. 4, Ln. 30-67).

However, Lee fails to explicitly disclose converting the inputted analog data into a digital data throughout a gamma correction and providing the ramp signal which is adjusted for the gamma correction.

In the same field of endeavor, Tomoaki teaches an A/D converter for converting video analog to digital signal (abstract). Tomoaki further teaches that the A/D converter is capable of simultaneously executing gamma correction and A/D conversion in order to eliminate unnecessary external correction circuit and thereby reducing the cost. In light of the teaching from Tomoaki, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device of Lee to adjusts the ramp signal for a gamma correction in order to simultaneously executing gamma correction and A/D conversion as claimed by Tomoaki. The modification thus simplifying the circuit design and reducing the cost (Tomoaki: abstract).

With regarding to **claim 8**, Lee in view of Tomoaki discloses CMOS image sensor as recited in claim 7, wherein the converter means includes:

a CDS performing unit for performing the correlated double sampling to the inputted analog data (Lee: Fig. 5; Col. 3, Ln. 14-25; Col. 5, Ln. 51- Col. 6, Ln. 5); and

a comparison unit for receiving output of the CDS (Lee: Fig. 5) performing unit and the ramp signal to thereby perform the gamma correction (Tomoaki: abstract).

With regarding to **claim 9**, Lee in view of Tomoaki discloses the CMOS image sensor as recited in claim 8, wherein the gamma correction is performed in a digital signal basis (Tomoaki: abstract).

With regarding to **claim 13**, Lee in view of Tomoaki discloses the CMOS image sensor as recited in claim 7, wherein the ramp signal generator includes:

a plurality of capacitors and switches (Lee: Fig. 4A; capacitors C2 and CI1-CIM; switches S1-SM, T1-TM, SW1-SW4);

an amplifier (Lee: 401) coupled to the plurality of capacitors and switches, for receiving gain and reset voltages from an external circuit (Lee: see Fig. 4A; Col. 4, Ln. 58-67), and

a capacitance controller (Lee: SW4) coupled in parallel to at least one capacitor in the ramp signal generator in order to adjust the ramp signal (Lee: Col. 6, Ln. 25-50 wherein slope of the ramp are adjustable corresponding to the capacitors switching) for the gamma correction (Tomoaki: abstract).

With regarding to **claim 14**, Lee in view of Tomoaki discloses the CMOS image sensor as recited in claim 7, wherein the ramp signal generator includes:

a first switch connected to a gain voltage (Lee: Fig. 4A; switch S1 is coupled to V_GAIN);

a plurality of second switches connected in parallel to the first switch (Lee: Fig. 4A; see switches S2-SM);

a plurality of capacitors connected to the second switches (Lee: capacitors CI2-CIM are connected to Switches S2-SM respectively);

a third switch connected between the first switch and a ground voltage level (Lee: Switch T1 is connected between first switch S1 and Vss which is commonly used in the art as ground);

a fourth switch commonly connected to the plurality of capacitors and connected to a reset voltage (Lee: SW1 is connected between plurality of capacitors CI2-CIM and V_RESET);

a fifth switch connected to the plurality of capacitors (Lee: SW2 is coupled to capacitors CI2-CIM);

an amplifier for receiving the reset voltage and receiving the gain voltage via the filth switch for outputting a ramp signal (Lee: see the connections between V_RESET, V_GAIN, SW2, and amplifier 401);

a sixth switch connected in parallel to the amplifier (Lee: SW4); and

a capacitor connected in parallel to the sixth switch (Lee: C2).

With regarding to **claim 15**, Lee in view of Tomoaki discloses the CMOS image sensor as recited in claim 7, further comprising an output device for latching output of the converter (Lee: Fig. 3; storage 312; Col. 4, Ln. 22-24).

With regarding to **claim 16**, Lee in view of Tomoaki discloses the CMOS image sensor as recited in claim 15, wherein the output device includes:

an up-counter for counting a clock pulse (Lee: Fig. 3; counter 302);

a multiplexer for selectively transmitting a result of the up-counter in response to output of the converter (Lee: switch 308 which represents one of many other switches for other pixels, is interpreted as a multiplexer; Col. 4, Ln. 16-23); and

a latch for latching output of the multiplexer to feed a latched value to the multiplexer (Lee: Col. 4, Ln. 20-30).

8. Claims 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee in view of Tomoaki and further in view of Kinoshita (US-6150850).

With regarding to **claim 10**, Lee in view of Tomoaki discloses the CMOS image sensor as recited in claim 7, wherein the converter means includes:

the chopper comparator (Lee: Figs. 3-4A; comparators 310 or 401). However, Lee and Tomoaki fails to explicitly disclose chopper comparator of the converter includes:

a first switch for transmitting the inputted analog data to a first node;

a second switch for transmitting the ramp signal to the first node;

a first capacitor coupled to the second switch and the first node;

a first device for converting a value of the first node;

a second device for converting output of the first means; and

plural capacitors coupled to the first and second devices, each for storing an offset voltage.

In the same field of endeavor, Kinoshita teaches a chopper comparator comprising:

a first switch (Fig. 7; switch SW2 transmitting Ain signal) for transmitting the inputted analog data to a first node (P is interpreted as the first node; Col. 7, Ln. 30);

a second switch (Fig. 7; switch SW1 transmitting Vref signal) for transmitting the ramp signal to the first node (Col. 7, Ln. 34-40);

a first capacitor (Fig. 7; C1) coupled to the second switch (SW1) and the first node (see Fig. 7; node P);

a first device for converting a value of the first node (the first device is interpreted as switch SW3 and inverter INV1);

a second device for converting output of the first means (see Fig. 7 wherein second device is interpreted as switch SW4 and inverter INV2); and

plural capacitors coupled to the first and second devices (C1 and C2), each for storing an offset voltage (Col. 7, Ln. 40-55; it is inherent that C1/C2, each stores offset voltage as shown in Col. 3, Ln. 30-50). Kinoshita further teaches that the high speed reset at the second capacitor causes the offset voltage of the chopper comparator to reduce and thereby improving the operation speed and precision of the analog/digital conversion (Col. 10, Ln. 9-21).

In light of the teaching from Kinoshita, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device of Lee and Tomoaki to include the arrangement of the chopper comparator claimed by Kinoshita in order to provide an improved analog/digital converter with high speed and precision (Kinoshita: Col. 10, Ln. 9-21).

With regarding to **claim 11**, Lee in view of Tomoaki and further in view of Kinoshita discloses the CMOS image sensor as recited in claim 10, wherein each of the first and second devices includes an inverter and a switch (Kinoshita: first device comprises switch SW3 and inverter INV1; second device comprises switch SW4 and inverter INV2).

With regarding to **claim 12**, Lee in view of Tomoaki and further in view of Kinoshita discloses the CMOS image sensor as recited in claim 11, wherein the gamma correction is performed in an analog signal basis (Tomoaki: abstract).

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hung H. Lam whose telephone number is 571-272-7367. The examiner can normally be reached on Monday - Friday 8AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Ometz can be reached on 571-272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HL

11/10/05

DAVID L. OMETZ
SUPERVISORY PATENT
EXAMINER